ABSTRACT OF THE DISCLOSURE

A semiconductor memory includes a Y decoder (1) and an X decoder (2). The Y decoder (1) is connected to two bit lines (3, 4), and the X decoder (2) is connected to four word lines (5-8). The drain terminals of flash memory cells (9-16) are respectively connected to one of the bit lines (3, 4). The bit lines (3, 4) are connected to a sense amplifier for detecting variations in voltage (or current) applied to the bit lines (3, 4) at the time of readout. The gate terminals of the flash memory cells (9-16) are respectively connected to one of the word lines (5-8). Further, bit line disconnecting transistors (17, 18) serving as disconnecting devices are provided between the Y decoder (1) and the bit lines (3, 4), respectively. The gate terminals of the bit line disconnecting transistors (17, 18) are connected in common.